

Training questions – Nanoelectronics

Single ANSWER is correct.

Q1. Which statement best describes the electrostatics of FinFETs?

1. The channel is fully wrapped by the gate on three sides, leading to stronger control.
2. FinFETs have higher parasitic capacitance than planar MOSFETs of the same area.
3. The fin height has no influence on the effective channel width.
4. FinFETs require heavy channel doping to control short-channel effects.

Q2. The use of ultra-thin-body FD-SOI reduces short-channel effects mainly because:

1. The buried oxide acts as a charge reservoir.
2. The depletion region spans the entire film, reducing the body potential.
3. The film thickness increases drain coupling.
4. The transistor operates in accumulation mode.

Q3. In Tunnel FETs, current conduction is dominated by:

1. Avalanche breakdown.
2. Drift-diffusion transport in the channel.
3. Band-to-band tunneling across a reverse-biased p-i-n junction.
4. Thermionic emission over a barrier.

Q4. A tunnel FET implemented on FD SOI substrate:

1. Has a higher I_{off} than when implemented on a FinFET with same thickness and gate length.
2. Has a higher I_{on} current than when implemented on a FinFET with same thickness and gate length.
3. Has better resistance to radiation than a FinFET Tunnel FET.
4. Has less temperature dependence than when implemented on a FinFET with same thickness and gate length.

Q5. A homojunction Tunnel FET using a high-k gate dielectric for the gate control:

1. Can simultaneously increase I_{on} and reduce I_{off} compared to a gate with medium-k dielectric.
2. Can simultaneously increase I_{on} and reduce SS.
3. Has no temperature dependence.
4. Can have larger I_{on} current than a MOSFET with same channel dimensions at voltages higher than the threshold voltage.